

Development of Gallium Arsenide High-Speed, Low-Power Serial Parallel Interface Modules

Final Report to:
National Aeronautics and Space Administration
Lewis Research Center

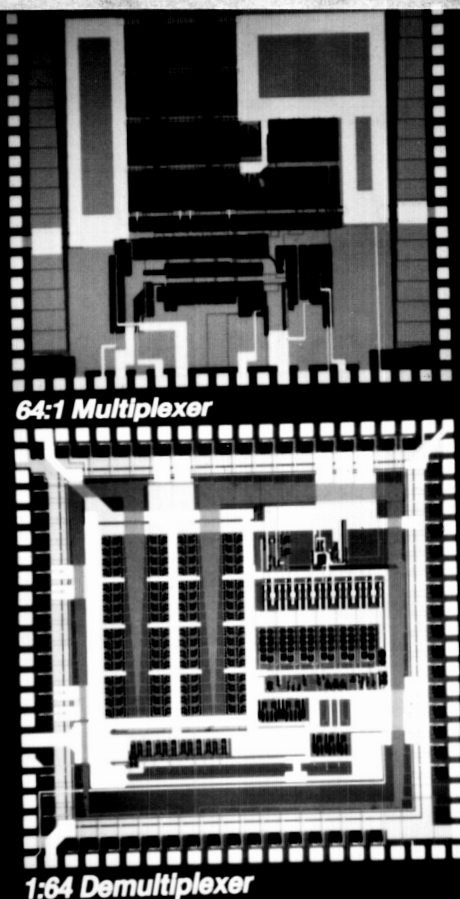
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NAS3-24676

(NASA-CR-182272) DEVELOPMENT OF GALLIUM
ARSENIDE HIGH-SPEED, LOW-POWER SERIAL
PARALLEL INTERFACE MODULES: EXECUTIVE
SUMMARY Final Report (Honeywell) 38 p

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Unclass
CSCI 09A G3/33 0198842



- High speed > 1.2 Gb/s.
low power consumption ~ 300 mW.
- Fabricated using Honeywell's submicron SAG E/D MESFET process. High yield demonstrated; 50% DC functionality.
- Low speed outputs TTL/CMOS compatible.
- 1100 gates for 64:1 multiplexers.
1500 gates for 1:64 demultiplexers.

Executive Summary

**Final Report to
National Aeronautics and Space Administration/
Lewis Research Center
for**

**DEVELOPMENT OF GALLIUM ARSENIDE
HIGH-SPEED, LOW-POWER
SERIAL PARALLEL INTERFACE MODULES**

Contract No. NAS3-24676

31 May 1988

Executive Summary

**Sensors and Signal Processing Laboratory
10701 Lyndale Avenue South
Bloomington, Minnesota 55420**

Honeywell Inc.

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SECTION 1

PROGRAM SCOPE AND GOALS

1.1 Background

This NASA Lewis program was funded as a 36 month program to develop a family of high speed, low power serial parallel interface modules. The program objective was to develop successfully higher speed-power performance using the emerging GaAs technology. Figure 1.1 shows the device performance goals required by the program. To achieve these goals, Honeywell proposed and is using a self aligned gate (SAG) MESFET technology developed at the Honeywell Sensors and Signal Processing Laboratory (SSPL) in Bloomington, Minnesota.

The program organization and overall schedule are shown in Figures 1.2 and 1.3, calling out the critical program personnel and the program major milestones.

Figure 1.4 summarizes the major program tasks to develop the device. The program costs were within the NASA authorized amount.

The work on this program has met the NASA Lewis speed-power requirements for the converters and more than the minimum quantity of 20 each devices have been delivered. This work was done within the cost and schedule goals of the program.

The following sections summarize the technical approach to develop the NASA serial-parallel converters.

The enhanced MESFET and advanced GaAs activity reported here was carried out separate from NASA funding.

Figure 1-1

PROGRAM GOALS

- o 16:1/1:16 Converter**
 - 100 MHz**
 - 100 mW**

- o 32:1/1:32 Converter**
 - 200 MHz**
 - 150 mW**

- o 64:1/1:64 Converters**
 - 550 MHz**
 - 250 mW**

- o Parts Deliverable**
 - 120 packaged parts**

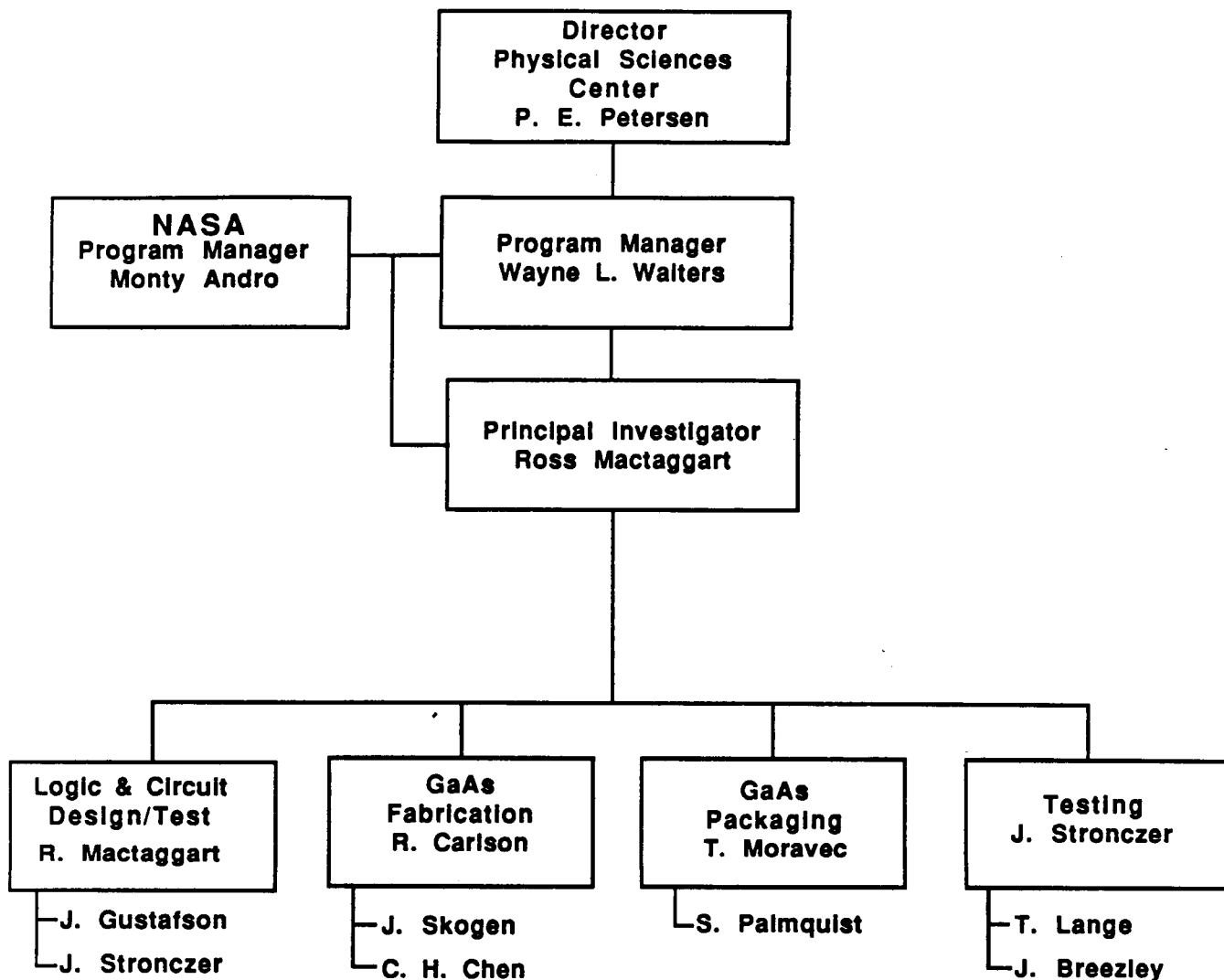


Figure 1.2 GaAs serial parallel program organization.

NASA 64:1 Program

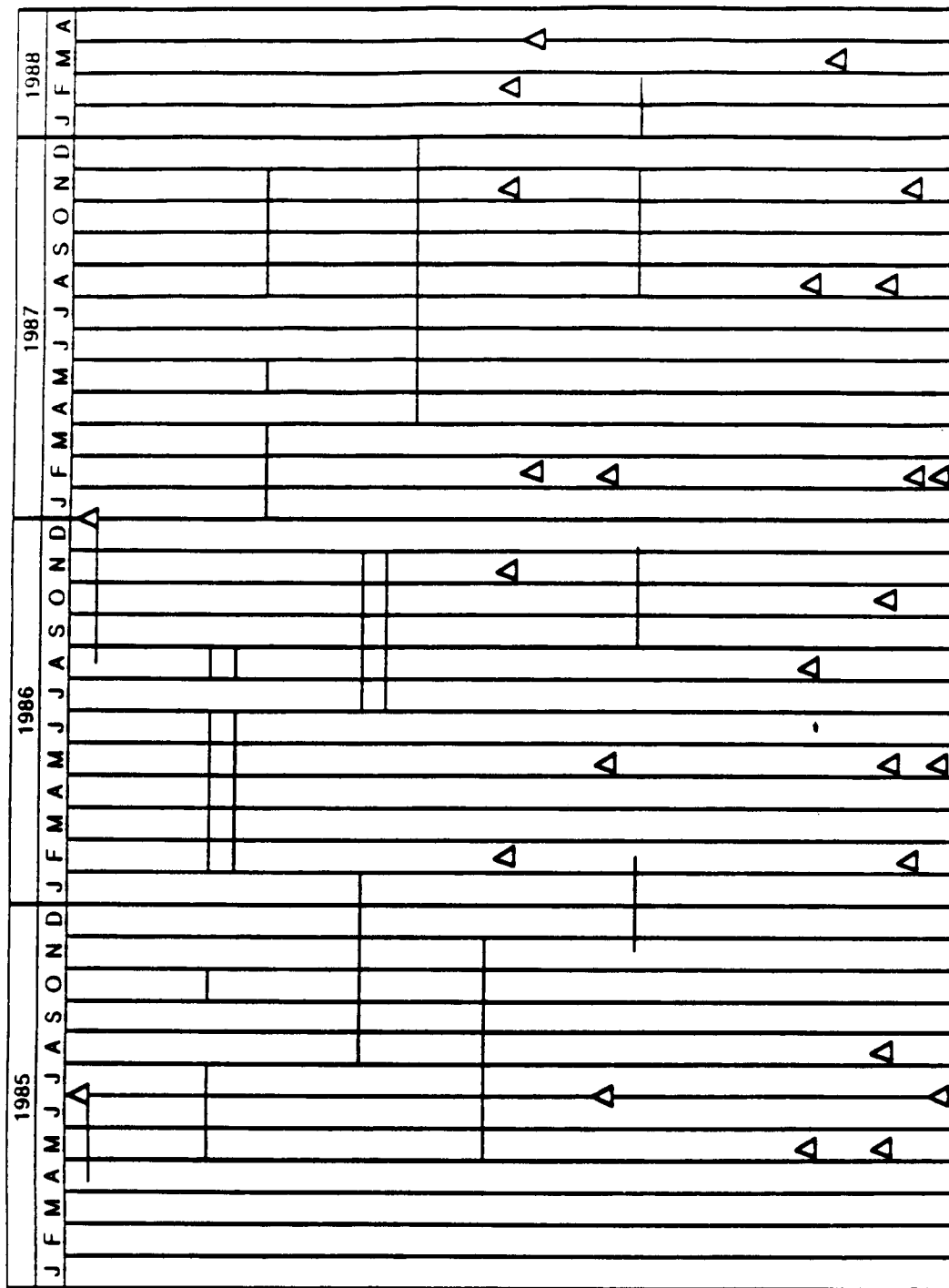


Figure 1.3

Figure 1.4

PROGRAM SCOPE

- o Design and Layout**
 - 16, 32 and 64 bit S/P, P/S
 - . 1 and 1.5 μ gate lengths
- o Processing**
 - SAG MESFET process
 - 2 passes of 16 and 32 bit devices
 - 1 pass 64 bit devices
- o Packaging**
 - Developed test fixtures for 16 and 32 bit
 - Packaged devices in flat packs
- o Testing**
 - Wafer Level
 - Package
 - Temperature
 - Radiation

SECTION 2

TECHNICAL APPROACH

Circuit Design

There are several architectural approaches to Parallel - Serial (P-S) and Serial - Parallel (S-P) converter design. The simplest and most common design approach is to use N series connected D-type flip flops with "load-in" and "load-out" capability. This is conceptually simple (Figure 2.1), but where the number (N) of D-type flip flops is greater than 8 or 16, the timing becomes less strongly coupled between the clock and "load-in" and "load out" signals and optimum performance is difficult to achieve. This is because the "load-in" and "load-out" nodes require extensive buffering, thus increasing the potential timing error between these signals and the main "load-across" clock (clock in). This is not a problem with a small number of D-type flops (e.g. 4 or 8), but requires considerable care for 16, 32 and especially 64 bit functions. In addition, every D-type flop is required to clock at the full clock rate with the simple serial architecture.

An alternative approach to the design of P-S and S-P converters with large conversion ratios (16, 32 and 64:1) is to perform the P-S and S-P function in more than one stage. This allows one high speed stage to be followed by a slower stage or stages, thus simplifying the high speed timing by limiting the number of flip-flops. The particular advantages that this approach offers is that:

- o Power consumption can be reduced
- o High speed timing is more tightly coupled to the high speed clock and is therefore easier to optimize.
- o Generic high speed "front end" can be built for a family of converters.

The specific approach chosen was a two stage up/down conversion using a generic high speed 4:1 and 1:4 multiplex and demultiplex function. Figures 2.2 and 2.3 shows block diagrams of the P-S and S-P architecture.

The low speed registers used an edge sensitive latch designed to consume about 700 μ W.

Figure 2.4a shows the logic used to construct this latch. A negative going edge will output the data set up from the data input. The high speed register and timing that was used is shown in Figure 2.4b.

Once the data has settled at the output of the low speed latches, the high speed latches load in data from the four bit wide bus (of the low speed latches). Immediately after this event, the low speed latches receive a clock event which provides a new four bit wide data word for the high speed latches. The high speed latches must load out 4 bits of data (serially) for every new four bit wide data word presented to it by the low speed latches. Thus, low speed latches operate at a frequency of $\text{clock} / 4$ and the high speed latches operate at the full clock rate.

De-multiplexer Operation

The de-multiplexer architecture is generic as was the case with the multiplexer. In the case of the de-multiplexer, a high speed generic 1:4 de-multiplexer stage was used. This produced a 4 bit wide bus with one quarter of the data rate. At this point edge sensitive latches were used to absorb the incoming data. As the clock rate is one quarter of the main clock rate, the timing on these latches is fairly non-critical and low power latches were used because of the low speed requirement.

Synchronization of the de-multiplexer was accomplished by setting the internal counter into a particular state as determined by the S_N bus (e.g. for the 16:1, S_0, S_1, S_2, S_3).

This event is initiated by a positive edge on the sync. input line known as First Word Bit Zero (FWB0). The counter then determines the load-out time, thus providing word synchronization. This sync event writes a logic "1" into a special latch which is reset to "0" several clock cycles later by a counter event. This produces a low speed recognition of the high speed synchronization event and is known as First Word Hold (FWH).

In addition, a divide by N (16, 32, or 64) output is provided. This is known as data-valid (DVD) and provides an indication as to when the output data bus should be sampled.

The high speed de-multiplexer registers are shown in Figure 2.5. The low speed register used was the same as that used in the multiplexer, which was an edge sensitive DFLOP with $700\mu W$ power consumption. High speed timing for the demultiplexer is very similar to the multiplexer and is not shown on the Figure.

Using this architecture approach, the 16-32 and 64 bit serial-parallel devices were designed for processing in the Honeywell MESFET GaAs technology. Figures 2-6 is of photo micrograph of the field containing the 16 and 32 bit devices. Each field contains 3 each 1-16/16-1's, and 2 each 1-32/32-1 devices. Figure 2-7 shows the 32 bit devices in more detail. The second pass design and layout was for the 64 bit devices and are shown on the cover and on Figure 2-8.

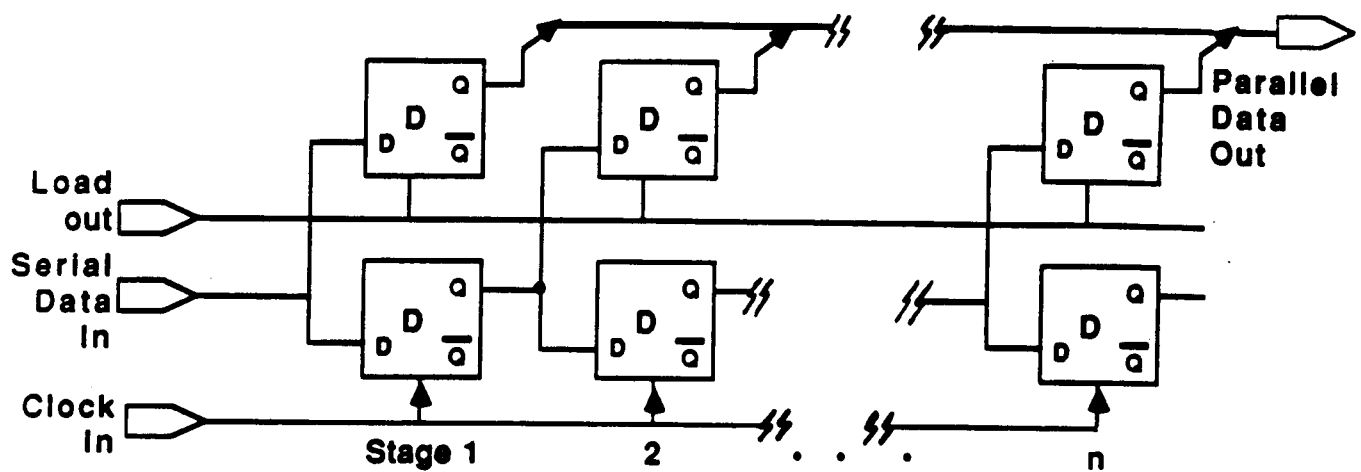
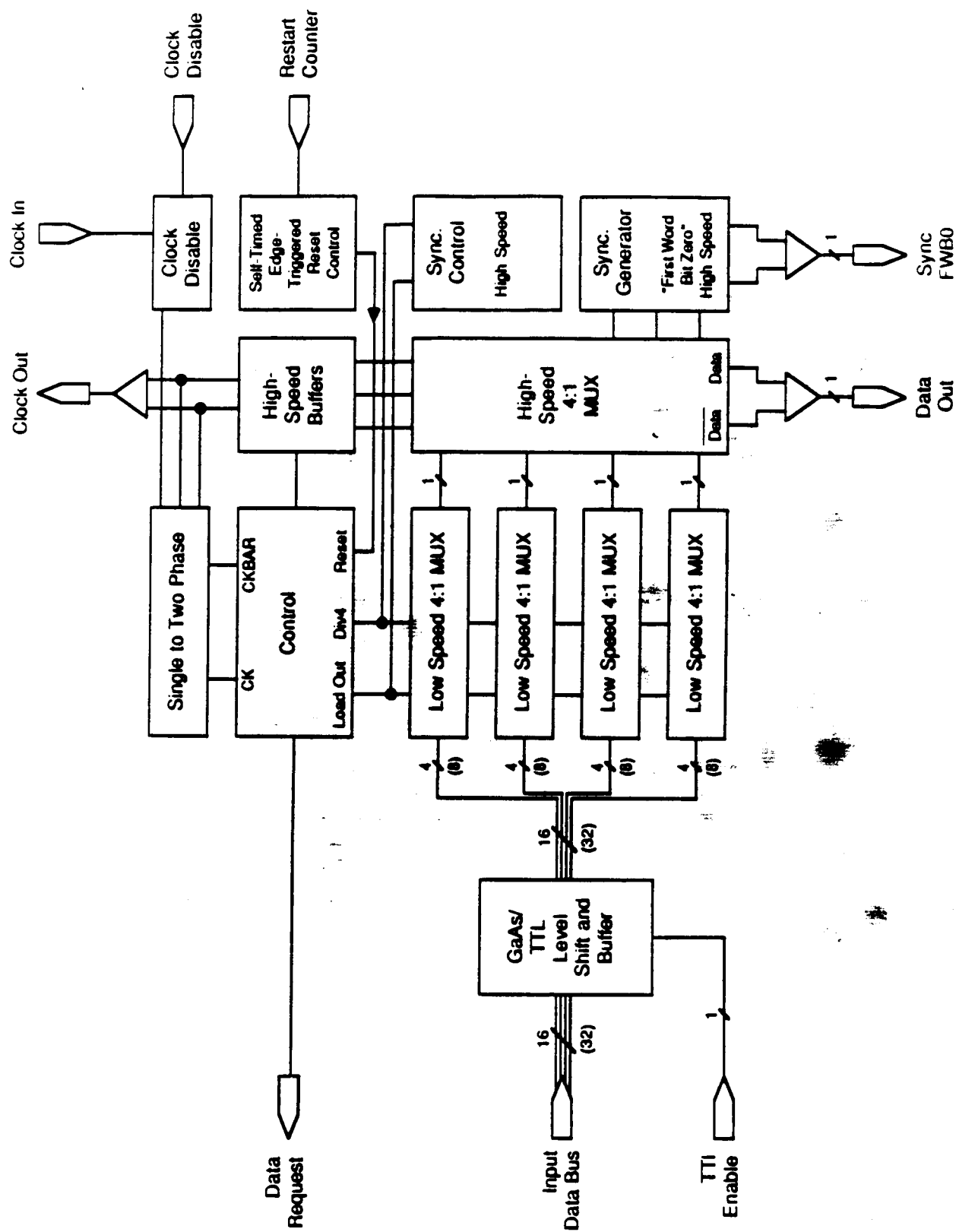
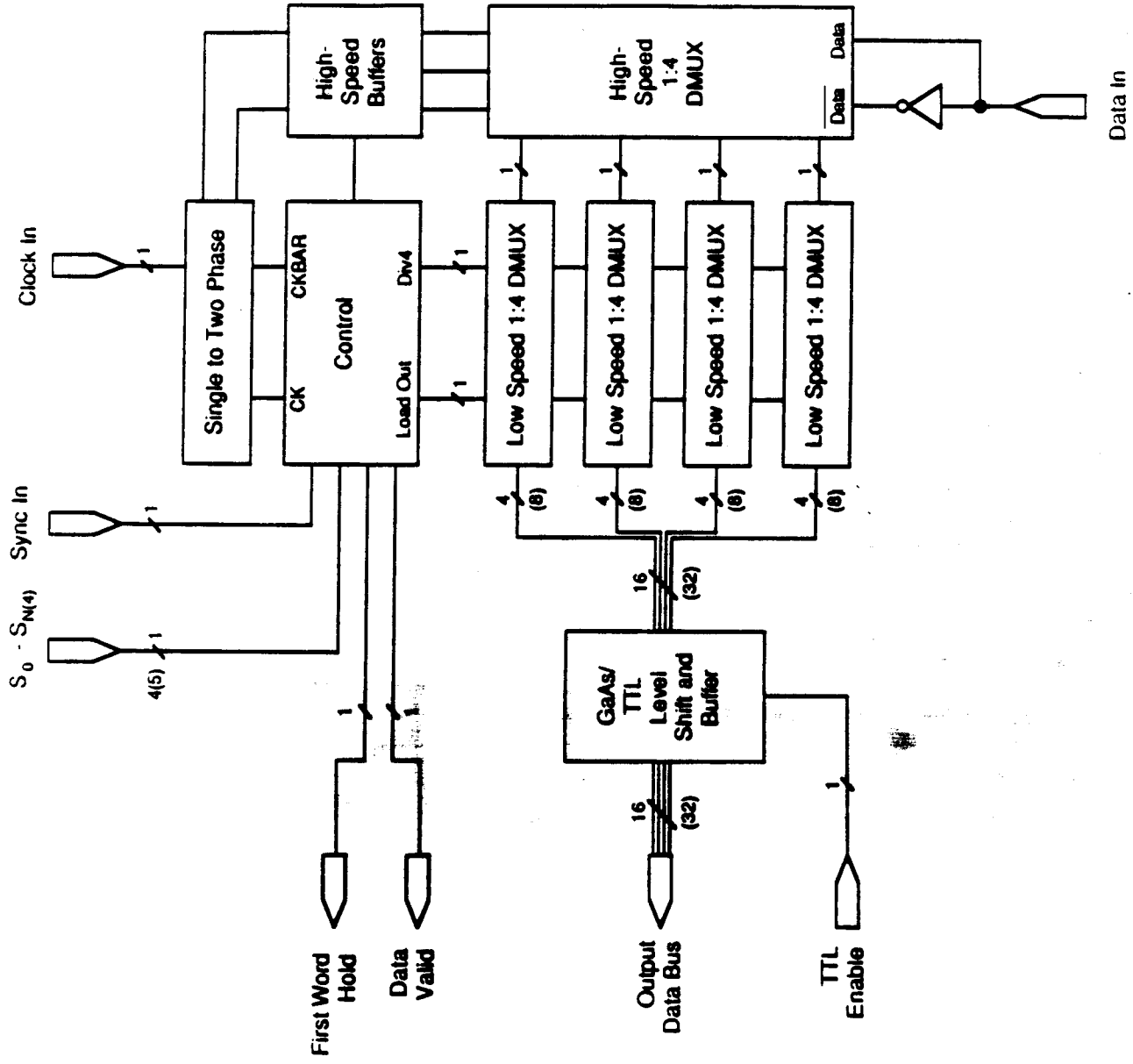


Figure 2.1 Simplest S-P converter using D-type flip flops.



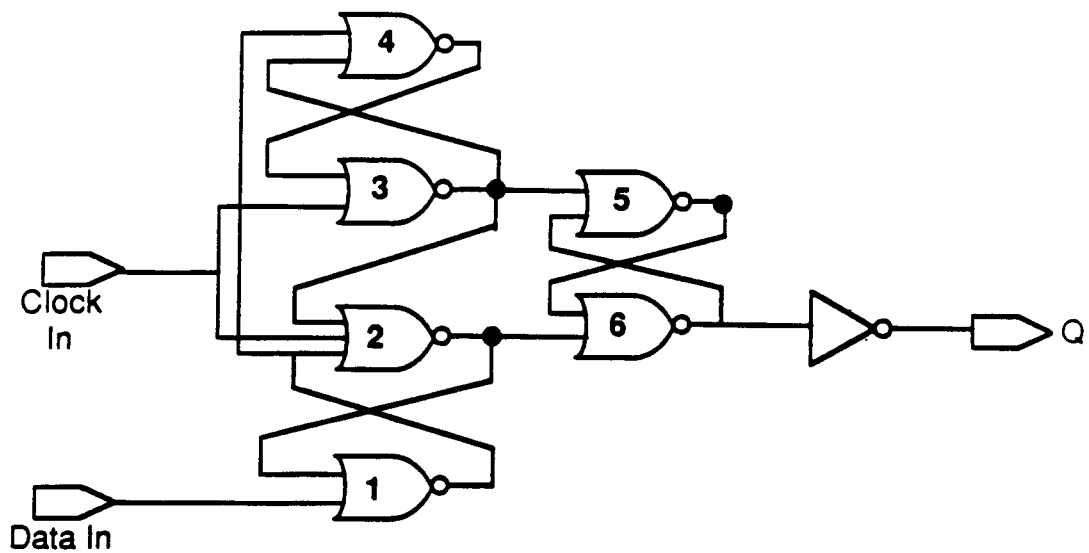
Generic Multiplexer Architecture Using High-Speed 4:1 Output Stage

Figure 2.2

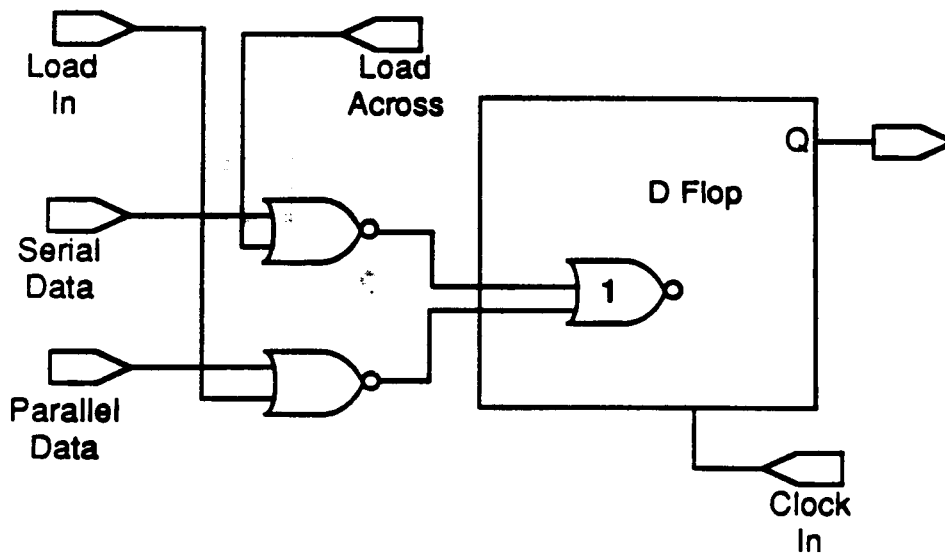


Generic Demultiplexer Architecture Using High-Speed 1:4 Input Stage

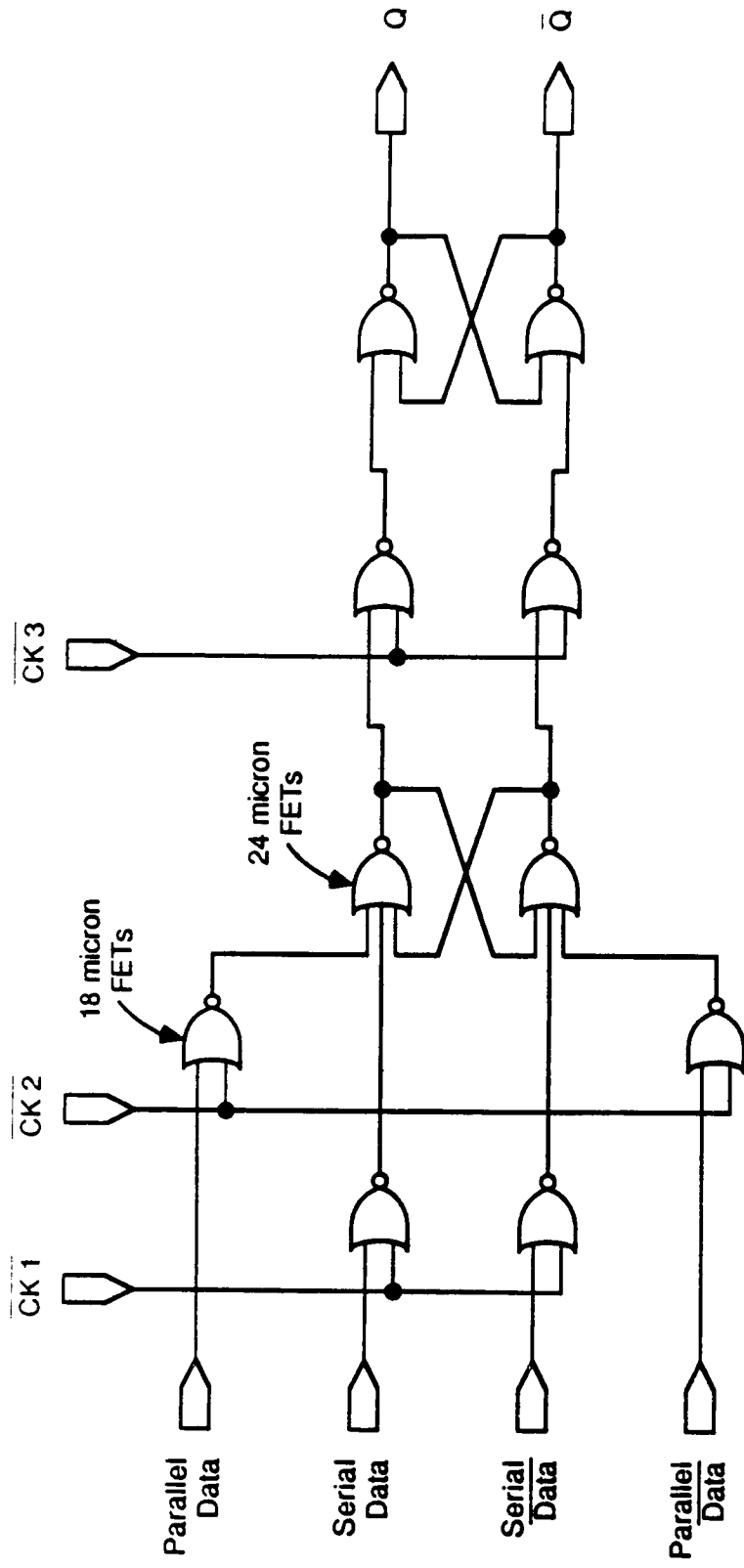
Figure 2.3



Edge sensitive latch for low speed circuits.



Low speed multiplexer stage.



High Speed 4:1 MUX Latch

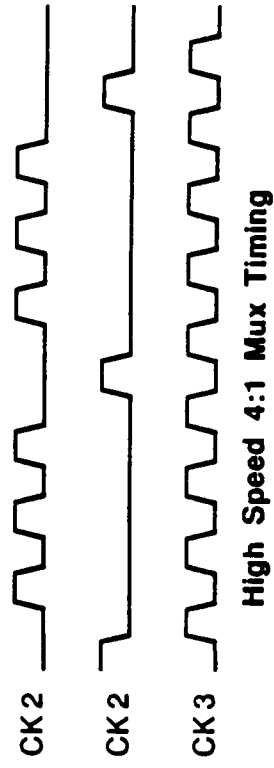
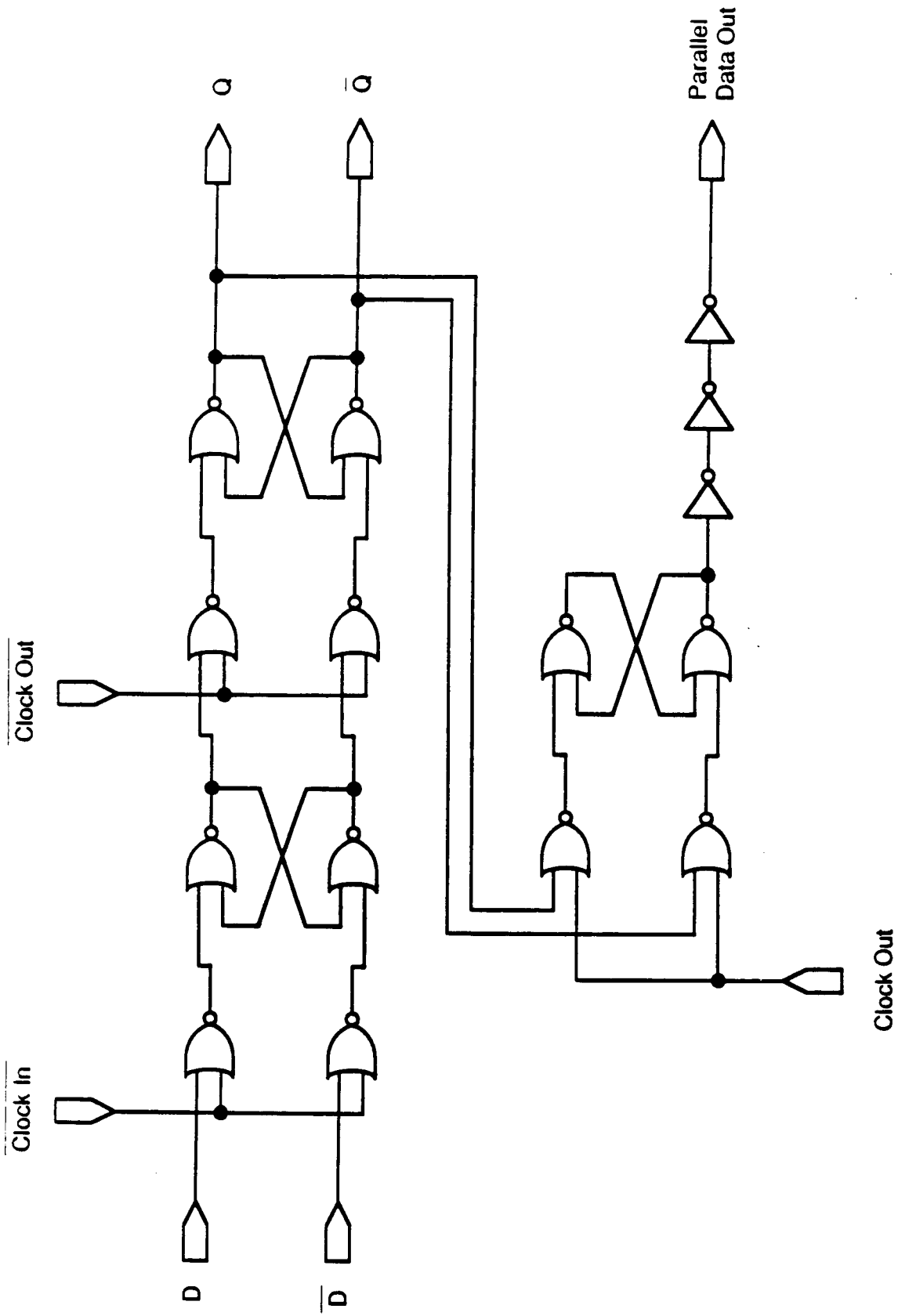


Figure 2.4 b)

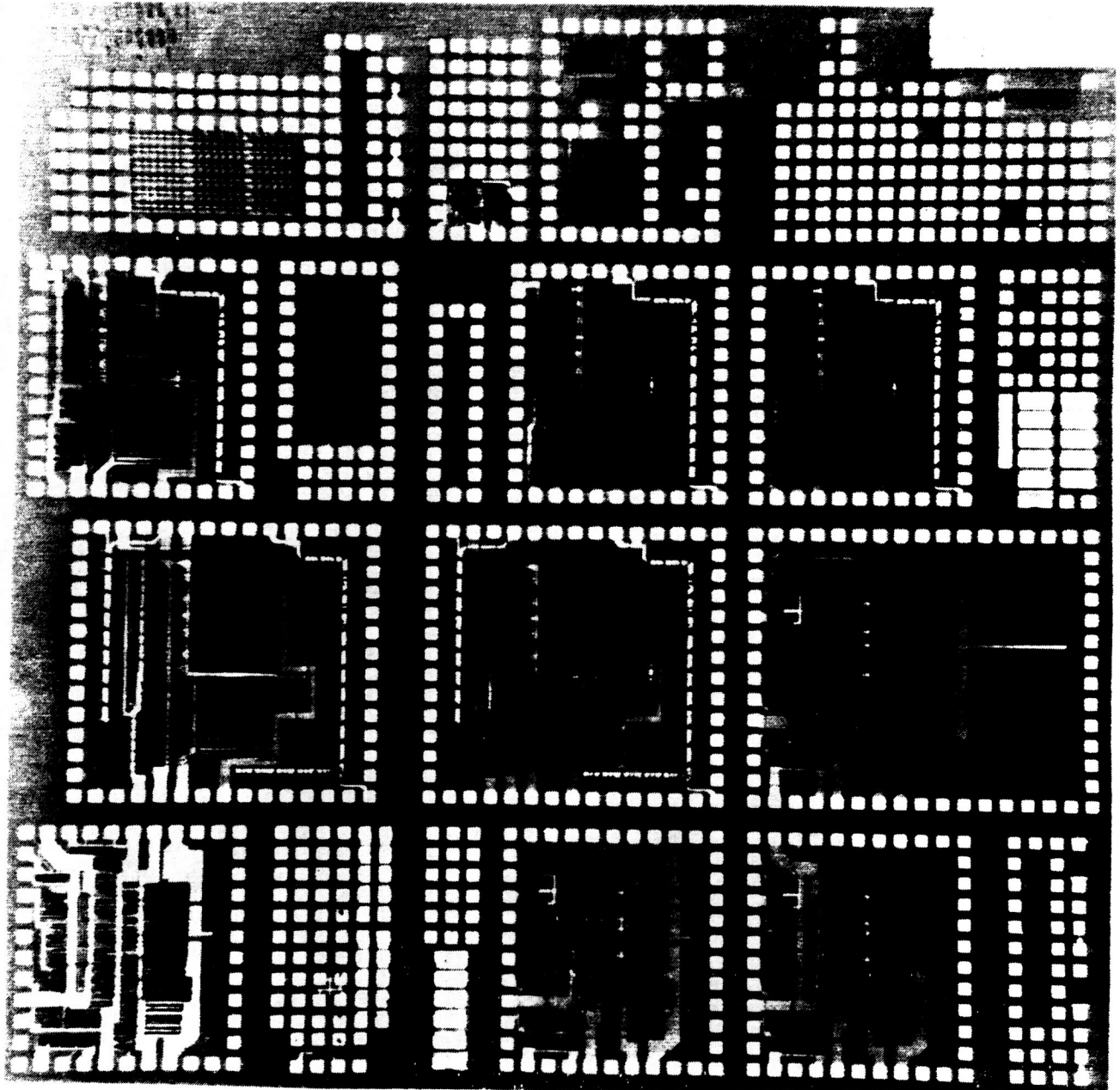


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High Speed Demultiplexer Registers
Used in 1:4 Front End for 16, 32, and 64 Bit Designs

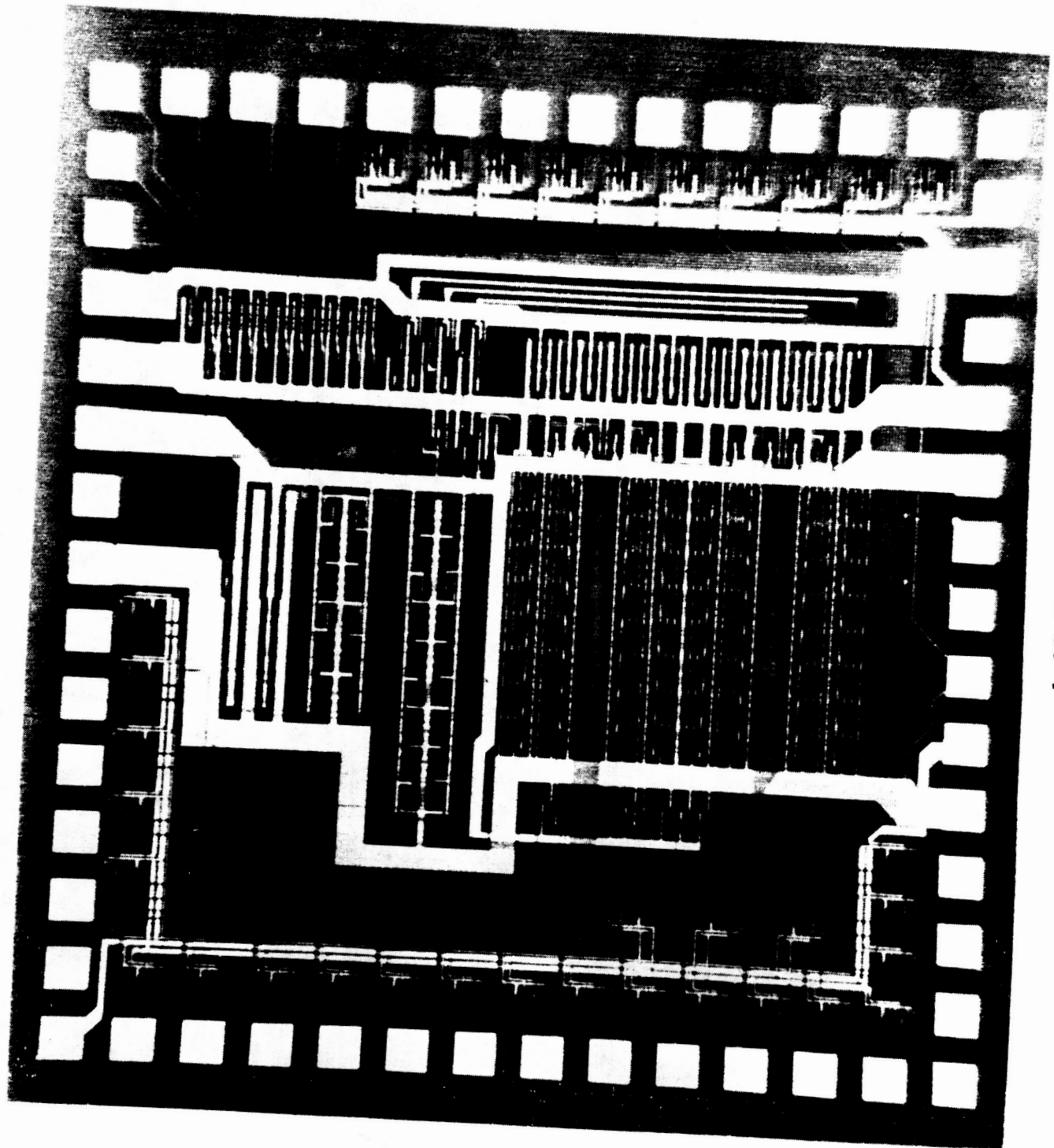
Figure 2.5

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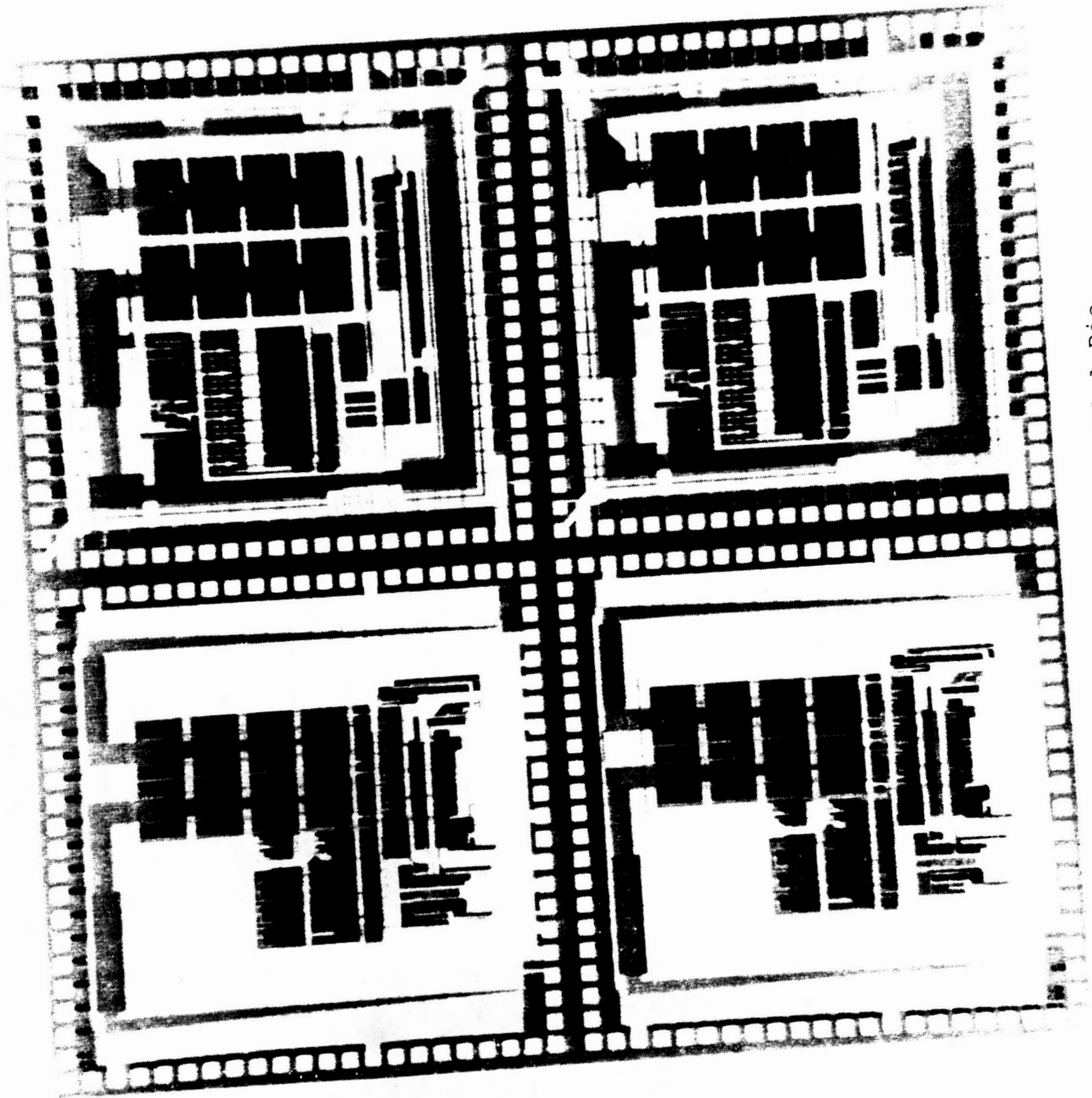
16 and 32 Bit Serial-Parallel
Converter Mask Set
Figure 2-6

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1:32 Multiplexer
Figure 2-7

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64 Bit Serial-Parallel Die
Figure 2-8

GaAs Processing

Honeywell's GaAs Self-Aligned Gate MESFET process is based on selective ion implantation into 3-inch GaAs substrates. Photolithography is accomplished using 10:1 a projection aligner with die-by-die alignment. A cross-sectional view of the wafer at various points in the fabrication process is shown in Figure 3-1.

The channel layer is implanted using a Si_3N_4 implant cap and then activated in a furnace oven. The anneal cap is stripped and the refractory metal gate is sputter-deposited and patterned using plasma etching. This gate metal then serves as the self-aligned implant mask for the source and drain implants of the FETs with photoresist masking outside the device areas. The N+ implant is annealed with a Si_3N_4 cap using a rapid optical annealer (ROA). Ohmic contacts are formed by evaporation using a AuGe based metal which is patterned by a lift-off process, then alloyed.

Interconnect metalization consists of two-level metals defined by a dielectric assisted liftoff (DAL) technique. This DAL process, together with filled vias for interlevel interconnect, allows complete planarity of the chip topology which is important in obtaining a high yield for LSI/VLSI fabrication. Both interconnect levels have sheet resistances less than 0.07 ohms square. This low sheet resistance provides for low IR drops and RC time constants in complex high-speed circuits. Figure 3-2 is a summary of the SAG MESFET process in place at Honeywell and used for this program.

A passivation process has been developed which maintains the circuit yield. The process which places very little stress on the wafers, is a polyimide process cured at either 250°C or 350°C. Pads are opened by reactive ion etching. Wafers are diced by sawing, the functional die removed and cleaned before bonding and packaging. Greater than 90% yield is routinely expected on the passivation, dicing, and packaging steps. This fabrication process has been successfully used in the fabrication of several MSI as well as LSI circuits, for both digital as well as analog applications (Fig. 3-3). 1K SRAM with access times as low as 1 nsec at a power consumption of 700 mW have been achieved. In addition, we have fabricated 5x5 multipliers and 16:1 MUX/DEMUXs with yields well over 50%. Yield as high as 72% was achieved on one wafer for 5x5 multipliers with a multiply time of 133 psec at a power dissipation of only 130 uW/gate for an average fan-out of 2.2.

In addition to Honeywell's baseline 1 μm gate length process, we have successfully developed a submicron process fully compatible to our self-aligned gate baseline process. Since intrinsic transconductance is inversely proportional to gate length, reducing the gate length is a logical approach for achieving ultra high speed devices. This submicron process is capable of fabrication of devices down to 0.5 μm with negligible short channel effects.

The limiting factor in shrinking gate lengths of any self-aligned gate process is short channel effects. The subthreshold leakage current in submicron MESFETs may be severe enough such that the devices never pinch off. This, together with poor threshold voltage control and uniformity, limited our previous baseline process to gate lengths of 0.8 μm .

However, using sidewall spacers, we have demonstrated excellent device characteristics with no appreciable short-channel effects down to gate lengths of 0.5 μm . Peak transconductance for E-mode FETs was as high as 299 mS/mm at a V_t of 0.08 V.

In addition to the threshold voltage uniformity, a high gate turn on voltage is essential for DCFL circuit operation over a useful temperature range as well as obtaining a reasonable yield in the LSI/VLSI range. WSi_x gates typically limits gate turn on to less than 0.65 V. We have investigated the use of WN_x gate process using reactive sputtering of tungsten in a nitrogen ambient background. By using an aluminum nitride as an anneal cap, we have achieved gate turn on as high as 0.77 V for a 1x10 μm FET. The WN_x gate process was incorporated into our baseline process during the course of this work.

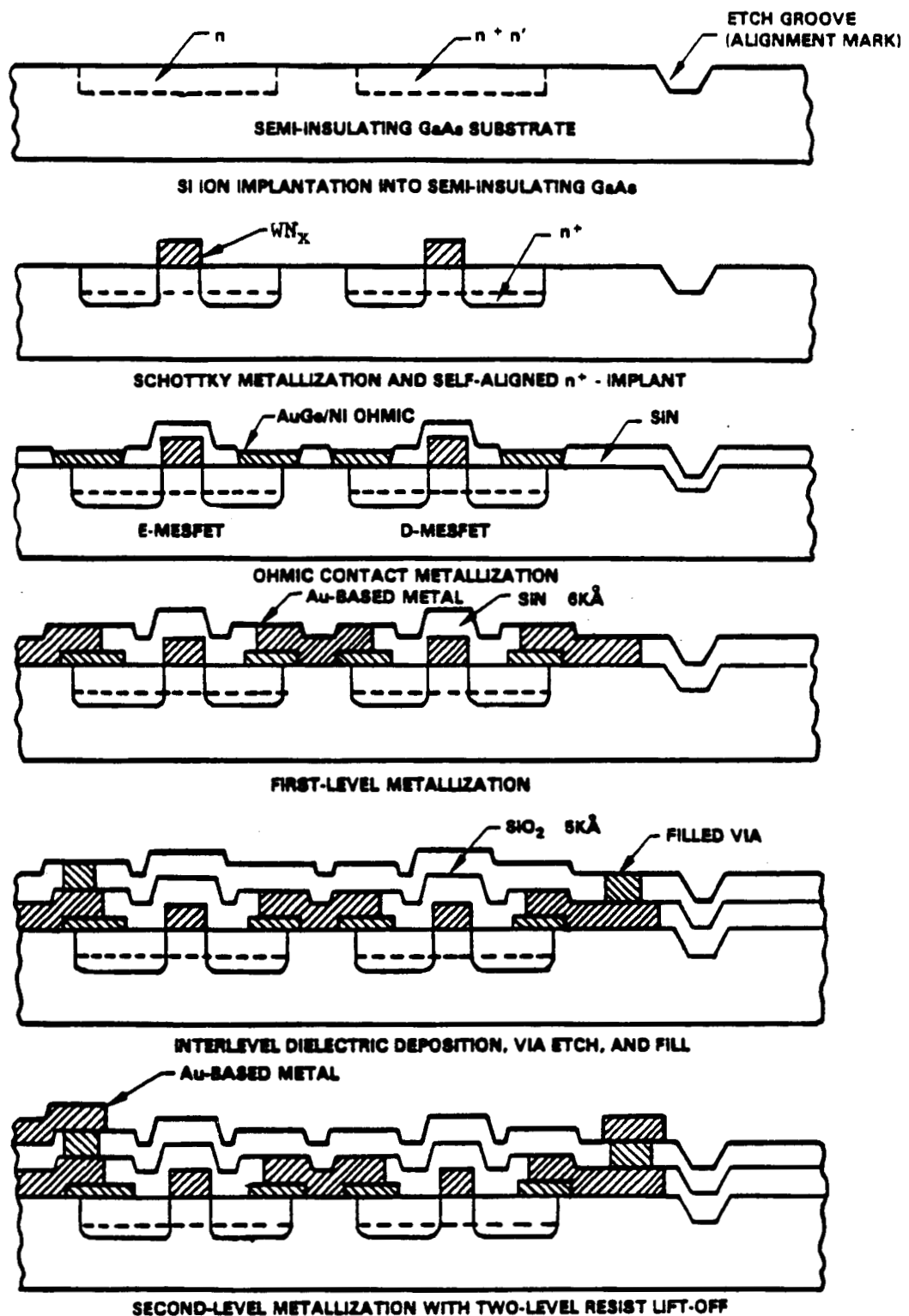


Figure 3-1 Cross-section of Honeywell's SAG E/D MESFET IC Process

Process Highlights

- o **10:1 Projection Lithography on 3 inch wafers**
- o **Self-Aligned Gate MESFETs with Refractory Metal Nitride**
- o **4 Micron Pitch for First and Second Level Metals Including Adjacent Vias**
- o **Resistivity of Both First and Second Level Metals Less Than 0.07 Ohms Per Square**
- o **Both Ohmic and First Level Metals Defined with a Dielectric Assisted Liftoff Process**
- o **Second Level Interconnect Defined by Two-Layer Resist Liftoff Process**
- o **High Yield Passivation Process. Low Loss Dicing and Bonding Verified.**
- o **Process Extendable to Three Level Interconnect System**

Figure 3-2

Key Recent GaAs Digital Circuit Results

- o **Self-Aligned Gate MESFET 5 x 5 Multiplier. 4 ns (133 ps/gate) at 39 mW (.13 mW/gate). 70% on-wafer yield.**
- o **MESFET 32:1 MUX and 1:32 DMUX ($L_g = 1.5\text{-micron}$). 450 MHz at 150 mW. 60% on-wafer yield.**
- o **MESFET 1K-Bit (256 x 4-Bit) SRAM. 1ns access time at 750 mW.**
- o **Submicron MESFET 1K-Bit SRAM. 1 ns access time at 400 mW.**

Figure 3-3

Packaging

The packaging requirements for this program are relatively modest, with the 550 Mbits/second being the highest speed for a data or clock line. This need can be met by careful assembly and installation of commercial flat pack style packages. Our test fixtures accomplish this while providing the required interface to test equipment.

There were six types of ICs developed in this program. Three package styles are used, one each for the 16-bit, 32-bit, and 64-bit chips. Four test fixtures were built for the 1:16, 16:1, 1:32, and 32:1 chip types. A single test fixture was sufficient for both 64-bit chips.

The highest speed signal in any package is 550 Mbit/second. This is a rather high digital data rate and requires that great care be exercised in guiding the propagation of the digital signals on and off the chip to the test equipment. However, it is not so high a data rate that a custom package with carefully designed transmission lines is required. We have found that at least one style of flatpack IC package has a construction closely resembling that of microstrip and stripline transmission lines. In our tests of this package style, we found that the typical VSWR of a line properly terminated inside the package was less than 2.0:1 up to about 3.5 GHz and less than 2.5:1 up to nearly 6 GHz. This indicates that the package is suitable for digital ICs with data rates exceeding 1 Gbit/second (assuming rise times of about .15 ns). Figure 4-1 shows an example of this VSWR test data.

The packages selected are Mini-Systems, Inc. flat packs. These packages have metal bottoms, which facilitates heat sinking and also improves the electrical ground for the data transmission lines. The die are attached with a silver epoxy (EPO-TEK H20E) with a 90°C cure temperature. The connection to the package leads is with 1-mil gold wire bonds. Bonding is preceded by a 5 minute O₂ plasma etch to clean all contacts. All ground contacts to the die are made to the package bottom. All high speed leads are surrounded by grounded leads, which are also wire bonded to the package bottom.

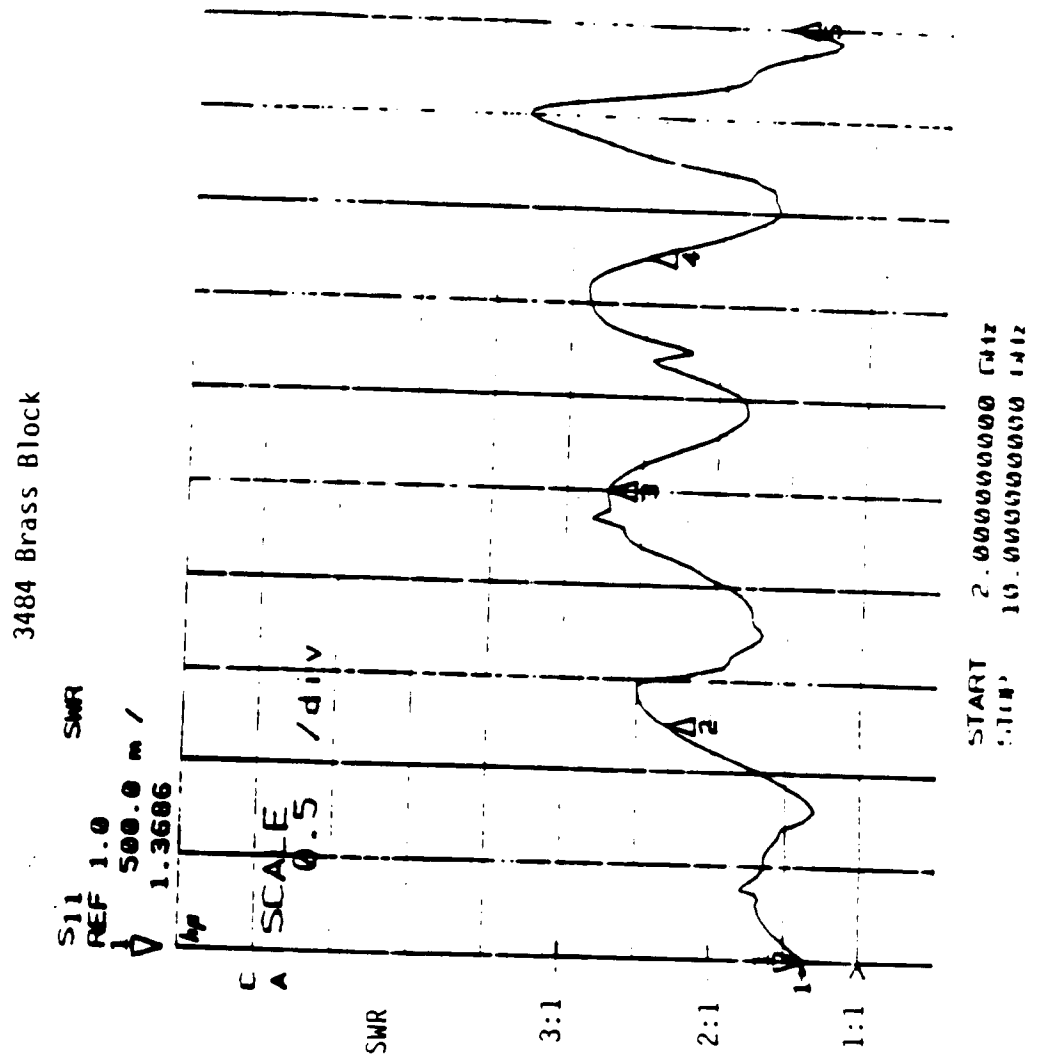
An additional advantage in using a commercial flat pack package is the relative ease of achieving a hermetic seal. Although our baseline approach of sealing the lid with silver epoxy is suitable for a laboratory environment, a hermetic seal is required for long-term reliability in more harsh environments. The hermetic seal is relatively easily

accomplished by soldering the lid to the package (along with the appropriate pre-seal bake and other preparation). Hermetic sealing was not used on this program since it had been untried and was considered an unnecessary risk to the NASA deliverables.

Figures 4-2 and 3 show the 32 and 64 bit devices in the flat packs. These devices were placed into specially developed test fixtures as shown in Figures 4-4 and 5.

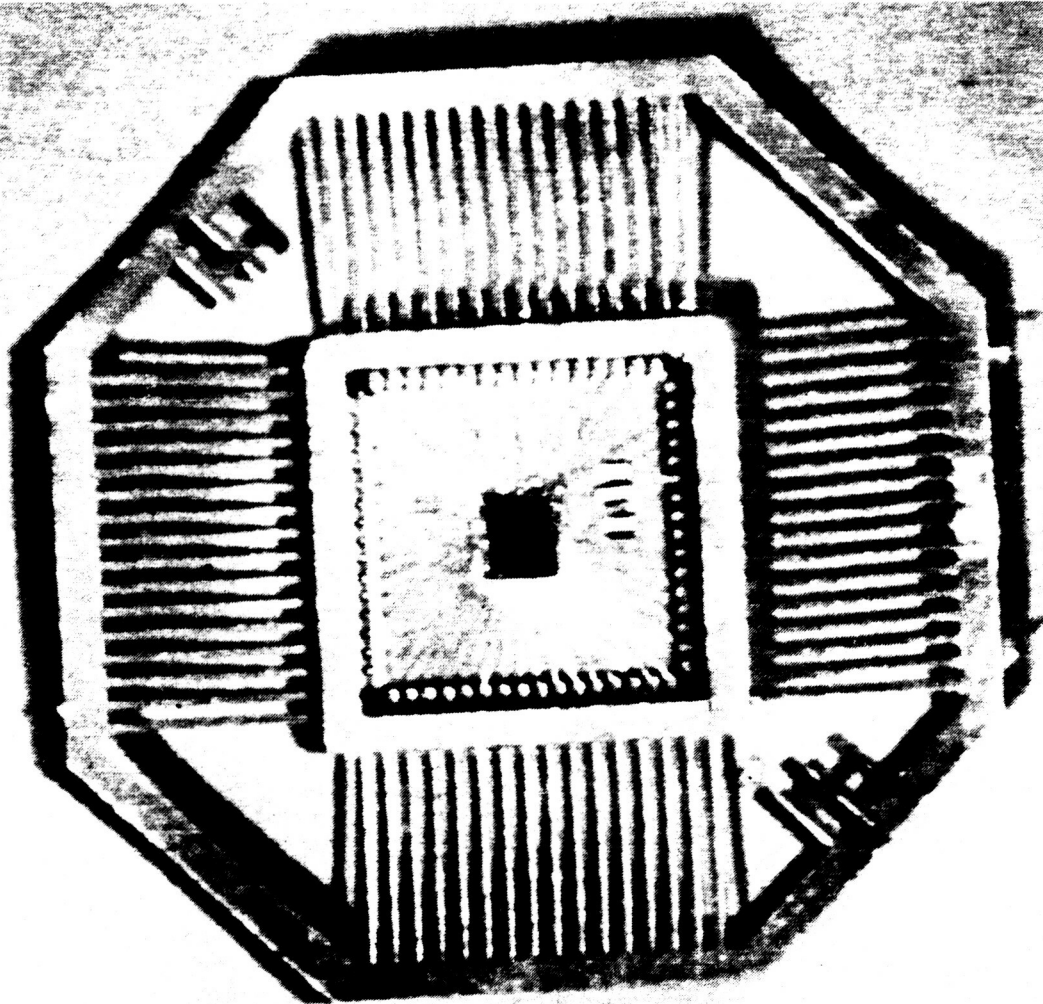
RETURN LOSS MEASUREMENT OF 84 LEAD FLATPACK

Figure 4-1



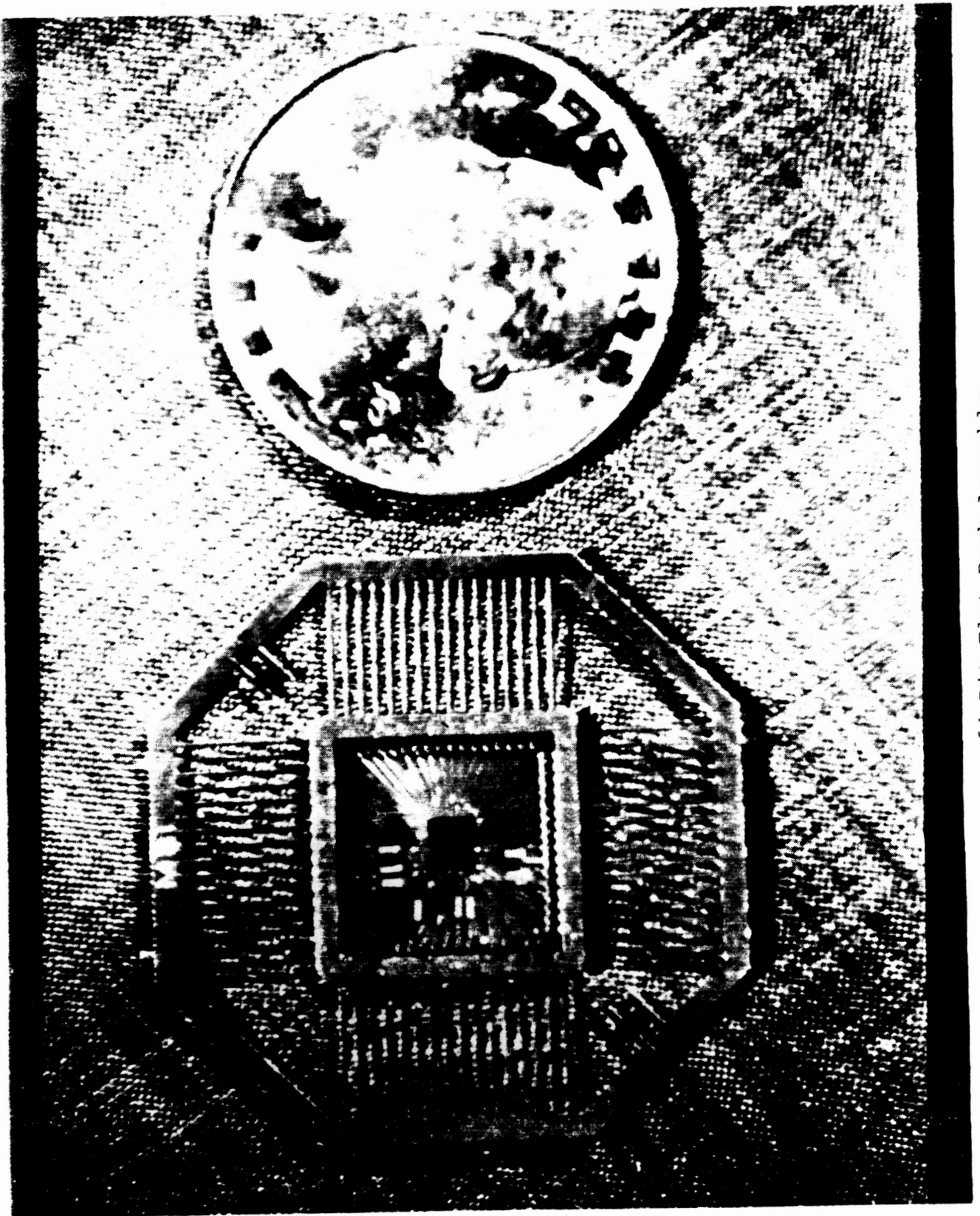
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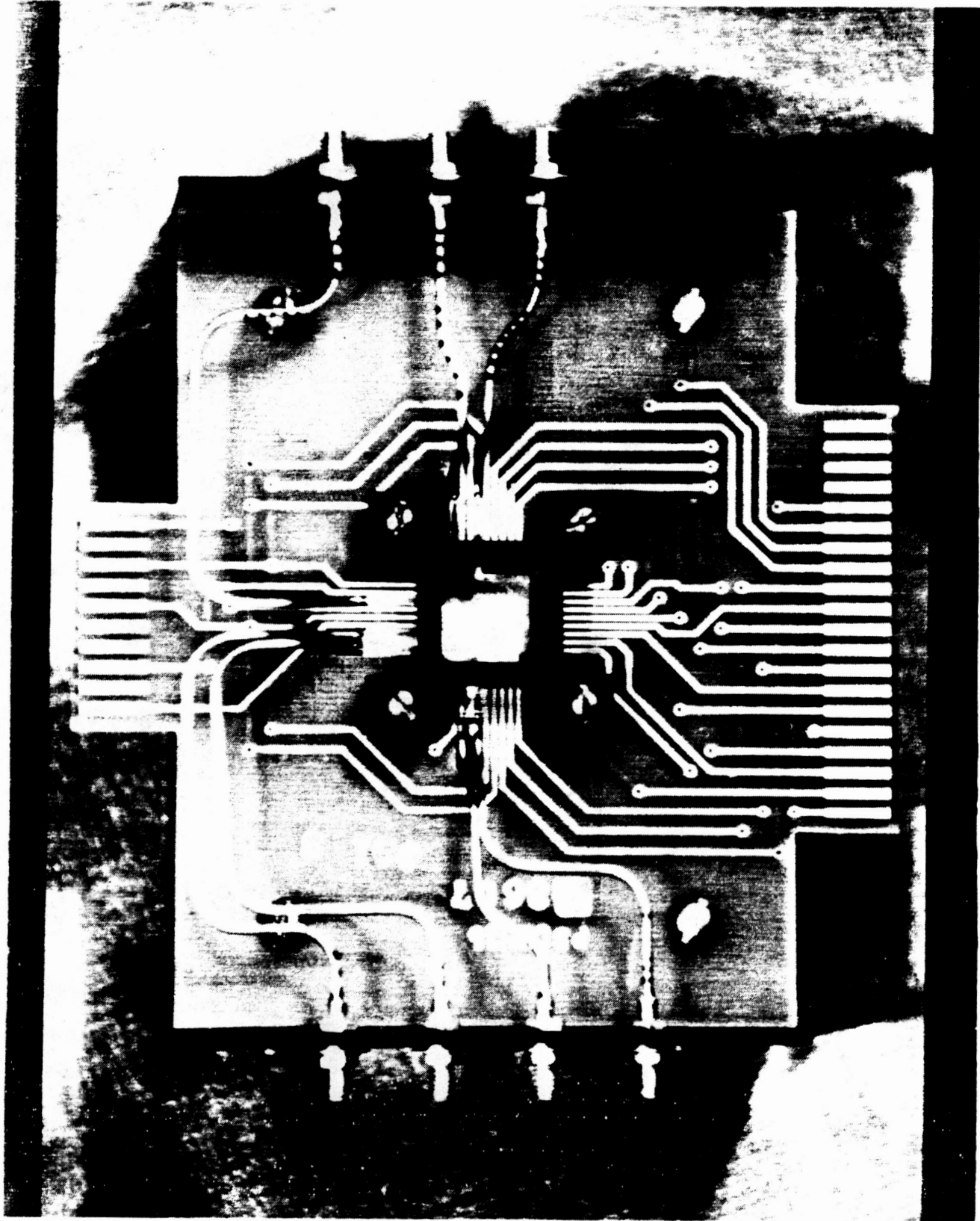
32 Bit FLAT PACK ASSEMBLY

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64 Bit Flat Pack Assembly
Figure 4-2

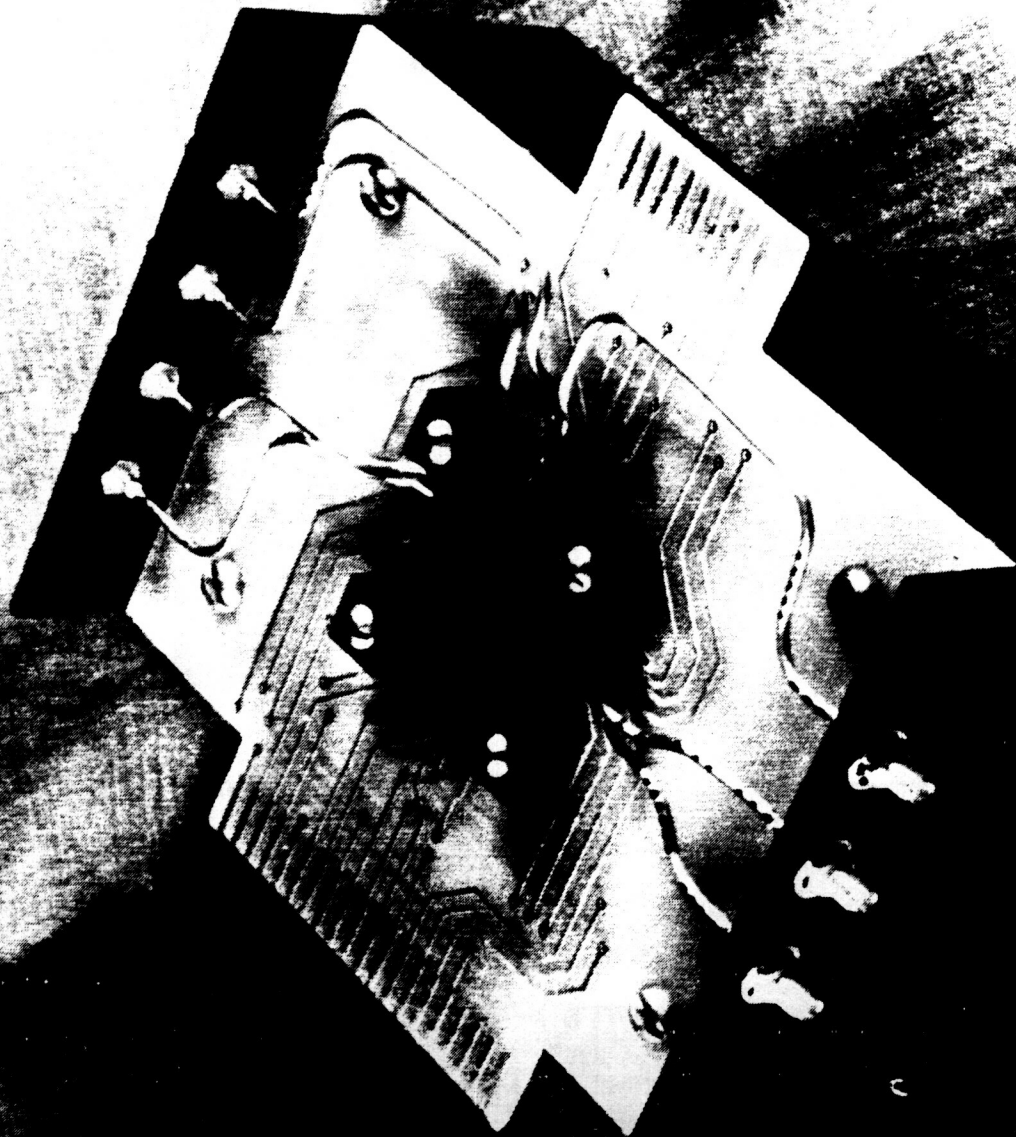
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16 Bit Test Fixture

Figure 4-4

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16 Bit Test Fixture

Figure 4-5

Testing

This testing involved a number of stages of increasing sophistication, starting with simple process parameter extraction and followed by functional testing. After functional testing at wafer level, chips were diced for bonding. This required that all six designs (16:1:16, 32:1:32 and 64:1:64) be fully functionally tested prior to bonding. Once the devices were bonded in the flatpacks, high speed testing was performed using the special test fixtures developed for the flatpacks. These allow high clock rates to be used up to 1000 MHz, if desired.

Low Speed Functional Testing

An IMS1000 pattern generator/data acquisition unit was used for wafer level testing. Some software was written for automatic wafer stepping. The functional testing consisted of performing a Restart (MUX) or Sync (DMUX) and then providing a stream of data designed to fully exercise all gates in the devices. As the devices have low gate counts, the number of vectors required need not be very large. Once the wafers were fully mapped, they were diced for bonding.

High Speed Testing

Some of the bonded wafers have been tested at high speed. The 16:1 devices yielded 200 to 400 MHz performance at 50-100 mW power consumption. A similar power figure was evident for the 1:16 devices. The 32:1 and 1:32 devices operated at the same speed with power about 20% higher than the 16 bit devices, i.e. about 60 to 120 mW. The 16:1 and 1:16 devices were connected in a high speed serial mode using the test fixtures and were demonstrated at 200 MHz including a synchronizaiton event at this speed.

Figure 5.1 shows the test set-up used. Figure 5.2 shows typical high speed test waveforms (data out and sync) together with a picture of a bonded 32:1 multiplexer.

Radiation Hardness (Honeywell Funded)

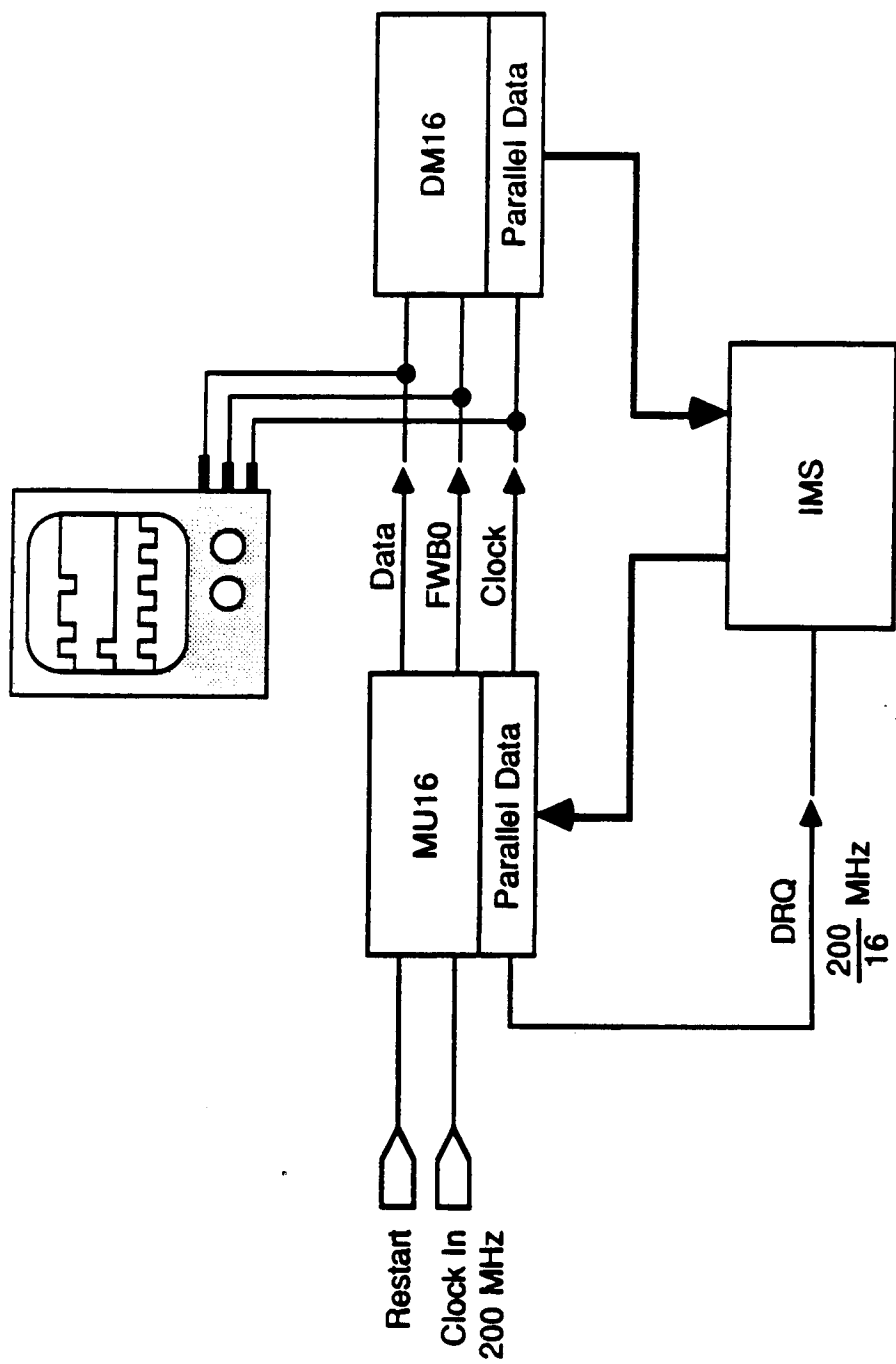
The 16:1 multiplexer was taken to Honeywell's Florida facility (SSAvD) and total dose testing was performed over a period of three days. After three days a failure occurred in the data out line. This corresponded to a 100 M Rad dose; however, a packaging

failure may have been responsible for this failure because a portion of the test fixture used partly disintegrated by the end of the test.

It was worth noting that the high speed SEN latch in the multiplexer did not get upset during the three day test, retaining the logic "1" set at the beginning of the test.

Temperature Testing

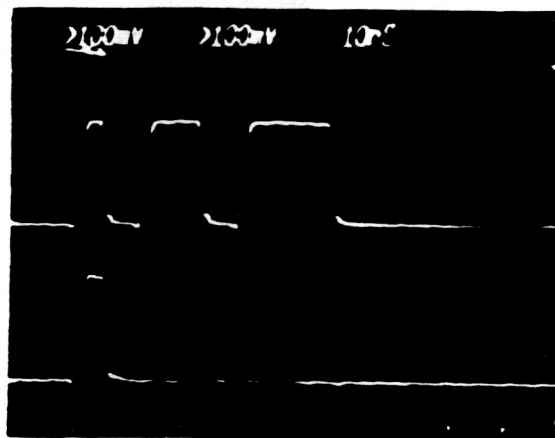
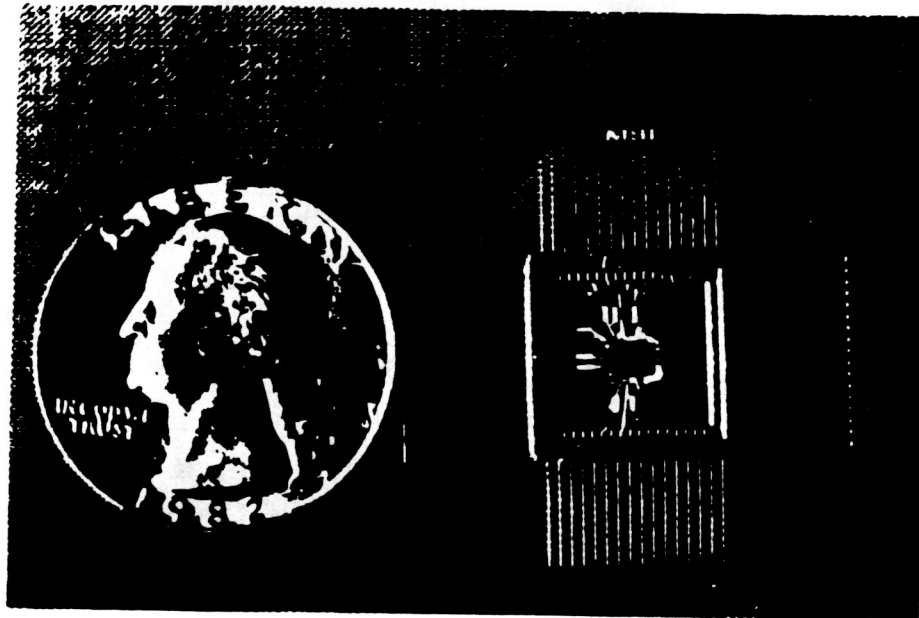
Two 16:1 multiplexers were bonded up and tested from room temperature to 180°C. Maximum clock rate increased slightly at the higher temperatures. Operation up to 140°C for one device and 168°C for the second device was measured. The deliverables have yet to be characterized at temperature extremes; however, they are likely to behave similarly to the devices measured from the first design pass.



**Test Configuration Using MUX and DMUX
to Verify High Speed Data Link**

Figure 5.1)

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Data Out
(1011011100000000)

Sync. Out

Power = 30mW at 1.0 volts
Speed = 200 MHz
Gate Length = 1.5 micron

Figure 5.2 High Speed Test Package and Waveforms

DELIVERED PARTS

	<u># Parts</u>	<u>Average Power mw</u>	<u>Nominal Speed MHz</u>
1:16	20	40	200
16:1	24	60	200
1:32	28	70	350
32:1	33	70	350
1:64	21	130	450
64:1	33	100	450

Figure 1-5

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15. Supplementary Notes Project Manager, Monty Andro, Space Electronics Division, NASA Lewis Research Center.					
16. Abstract Final report to NASA LeRC on the development of gallium arsenide (GaAs) high-speed, low power serial/parallel interface modules. The report discusses the development and test of a family of 16, 32 and 64 bit parallel to serial and serial to parallel integrated circuits using a self aligned gate MESFET technology developed at the Honeywell Sensors and Signal Processing Laboratory. Lab testing demonstrated 1.3 GHz clock rates at a power of 300 mW. This work was accomplished under contract number NAS3-24676.					
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